

Parametryzacja przetworników cyfrowo-analogowych

wersja: 02.2013

Cel ćwiczenia

Celem ćwiczenia jest zaprezentowanie istoty działania przetworników cyfrowo-analogowych (*DAC – digital-to-analog converter*), identyfikacja ewentualnych źródeł błędów przetwarzania, zdefiniowanie i pomiar podstawowych parametrów statycznych i dynamicznych przetworników DAC.

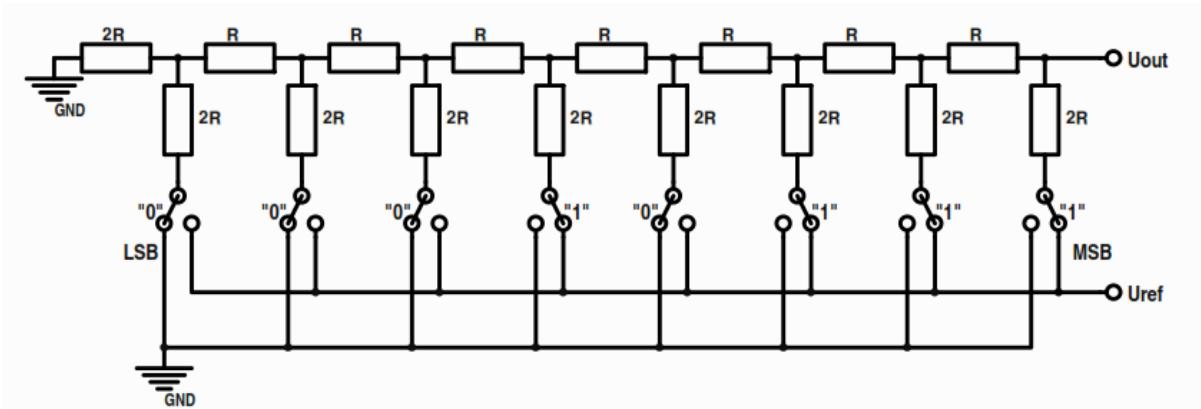
Program ćwiczenia

1. Pomiar liniowości 8-bitowego przetwornika cyfrowo-analogowego R-2R

Przetwornik cyfrowo-analogowy to układ w którym na podstawie wejściowego słowa bitowego *Data* i analogowego poziomu odniesienia *Ref* (napięcie lub prąd referencyjny) generowany jest analogowy sygnał wyjściowy:

$$U_{out} = Data * Ref$$

Schemat funkcjonalny przetwornika R-2R przedstawia rysunek poniżej:

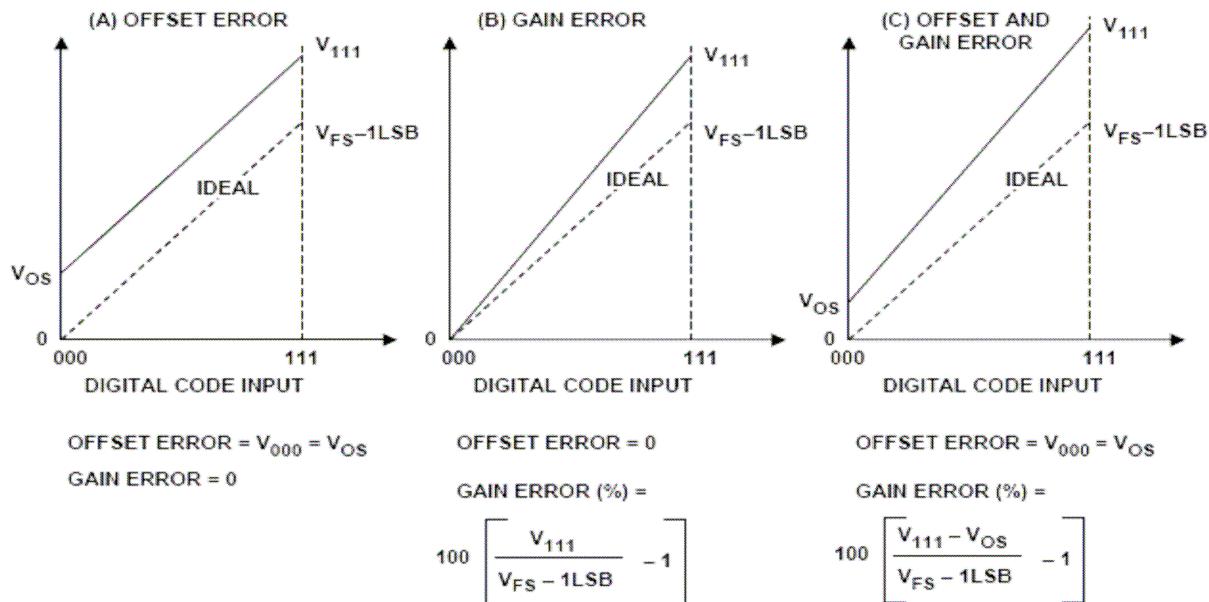


Rys. 1. Schemat funkcjonalny przetwornika cyfrowo-analogowego w konfiguracji R-2R.

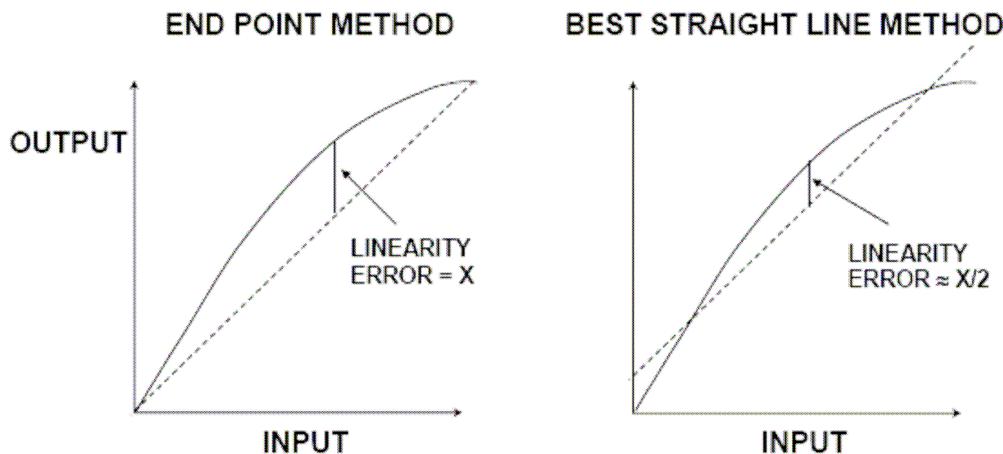
Rzeczywisty przetwornik cyfrowo-analogowy charakteryzuje się między innymi następującymi odstępstwami od charakterystyki idealnej:

- błąd przesunięcia zera,
- błąd wzmacnienia,
- błąd nieliniowości.

Odstępstwa te przedstawione są graficznie na rys. 2 i 3.

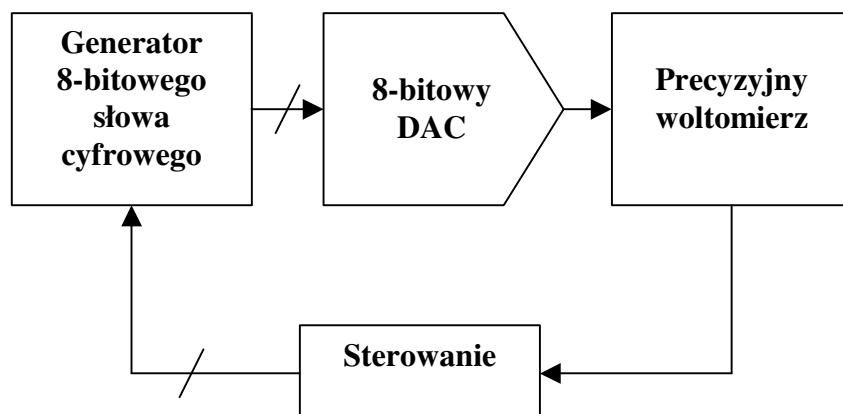


Rys. 2. Błędy rzeczywistego przetwornika cyfrowo-analogowego (zaczerpnięte z [6]).



Rys. 3. Błąd nieliniowości całkowej INL. Metoda wyznaczenia INL dla przetwornika DAC – a) metoda punktów końcowych, b) metoda najlepszego dopasowania analogowego (zaczerpnięte z [6]).

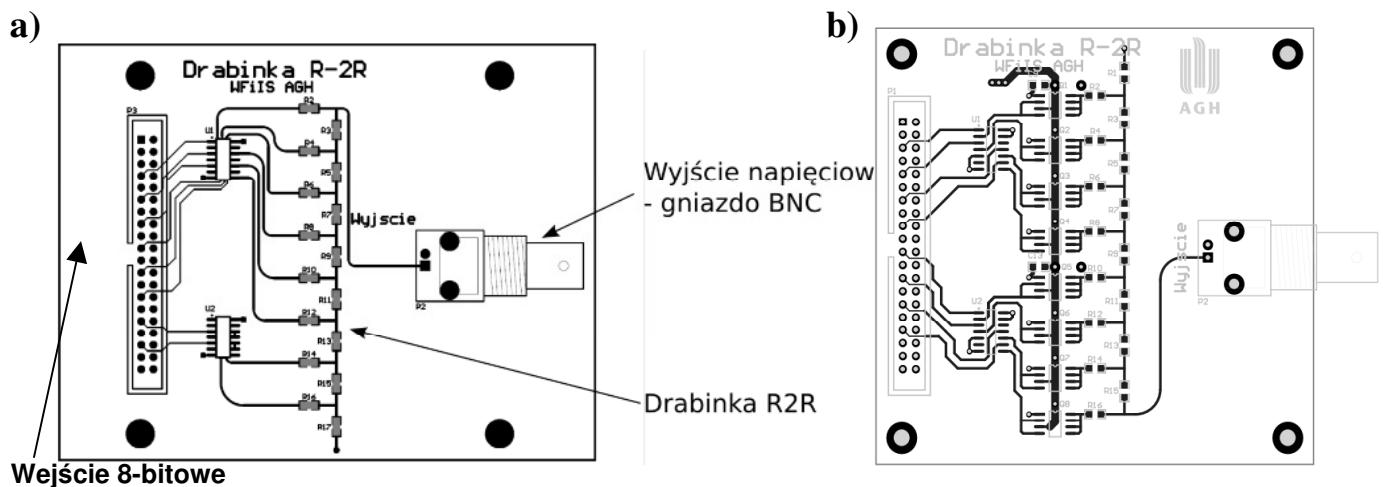
Do pomiarów stycznych wykorzystać należy poniżej przedstawiony schemat pomiarowy:



Rys. 4. Schemat blokowy statycznych pomiarów przetwornika DAC.

Podczas ćwiczenia przeprowadzony zostanie pomiar napięcia wyjściowego 8-bitowego przetwornika DAC w funkcji wszystkich wartości wejściowego słowa bitowego (od 0 do 255) dla jednej wartości napięcia referencyjnego.

Do ćwiczenia wykorzystać należy moduł rozszerzeń: *Przetwornik cyfrowo-analogowy R-2R* ćwiczenia laboratoryjnego *Programowalnych matryc logicznych – PLD*.



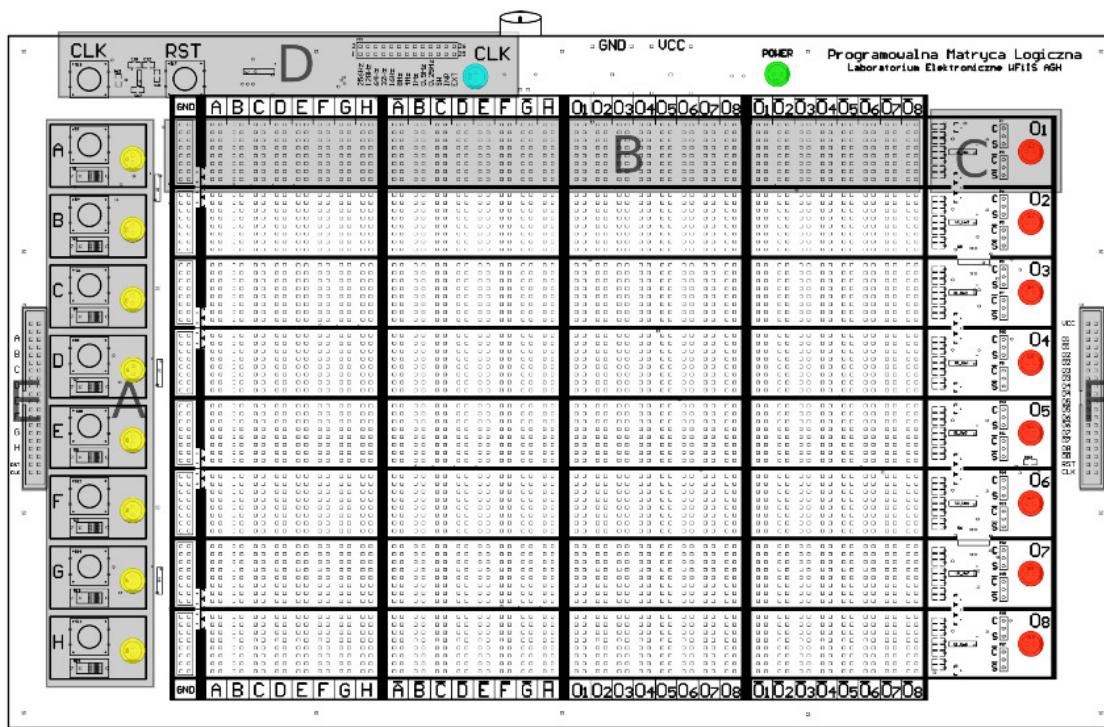
Rys. 5. Moduł rozszerzeń przetwornika DAC R-2R. Starsza wersja (a) i nowsza wersja (b) projektu płytki drukowanej.

W zależności od wariantu systemu pomiarowego wykorzystać można:

VARIANT 1:

- generator 8-bitowego słowa cyfrowego: odpowiednio przygotowana kasetka pomiarowa ćwiczenia laboratoryjnego *Programowalnych matryc logicznych – PLD* (opis poniżej),
- precyzyjny voltmierz: miernik uniwersalny *Agilent 34401A*,
- sterowanie: ręcznie lub automatycznie obsługiwana kasetka *PLD*.

Schemat blokowy *Programowalnych matryc logicznych – PLD* przedstawiony jest na rysunku 6. Grupą przełączników „A” ustawiane jest 8-bitowe słowo wejściowe. Poszczególne wejścia od A do H powinny być transformowane na złącze wyjściowe „F”. Do tego celu należy odpowiednio przygotować rozmieszczenie zworek programowalnego bloku logicznego „B”. Do złącza „F” podłączyć moduł rozszerzeń: *Przetwornik cyfrowo-analogowy R-2R*.



- A – Grupa przełączników do ustawiania sygnałów wejściowych
- B – Programowalny blok logiczny
- C – Zworki wyboru wejścia kombinacyjnego (C) lub sekwencyjnego (S) wraz z diodami sygnalizującymi stan wyjścia danego bloku logicznego
- D – Blok wyboru źródła sygnału zegarowego
- E – Złącze doprowadzające sygnały wejściowe
- F – Złącze wyprowadzające sygnały wyjściowe

Rys. 6. Budowa programowej matrycy logicznej – PLD [konspekt do ćwiczenia: Programowalnych matryc logicznych – PLD].

VARIANT 2:

- generator 8-bitowego słowa cyfrowego: karta cyfrowa NI USB-6008,
- precyzyjny woltomierz: miernik uniwersalny Agilent 34401A lub wejście analogowe karty NI USB-6008,
- sterowanie: komputer z oprogramowaniem sterującym w środowisku LabVIEW.

VARIANT 3:

- generator 8-bitowego słowa cyfrowego: generator przebiegów dowolnych AWG2021 firmy Tektronix,
- precyzyjny woltomierz: miernik uniwersalny Agilent 34401A,
- sterowanie: komputer z oprogramowaniem sterującym w środowisku LabVIEW.

Generator AWG2021 powinien pracować w trybie generacji przebiegu piłokształtnego o możliwie niskiej częstotliwości w opcji wyzwalania zewnętrznego. 8-bitowe słowo cyfrowe (osiem najbardziej znaczących bitów z 12-bitowej magistrali) uzyskiwane jest z wyjścia CH1 DIGITAL DATA OUT dostępnego w tylniej części obudowy.

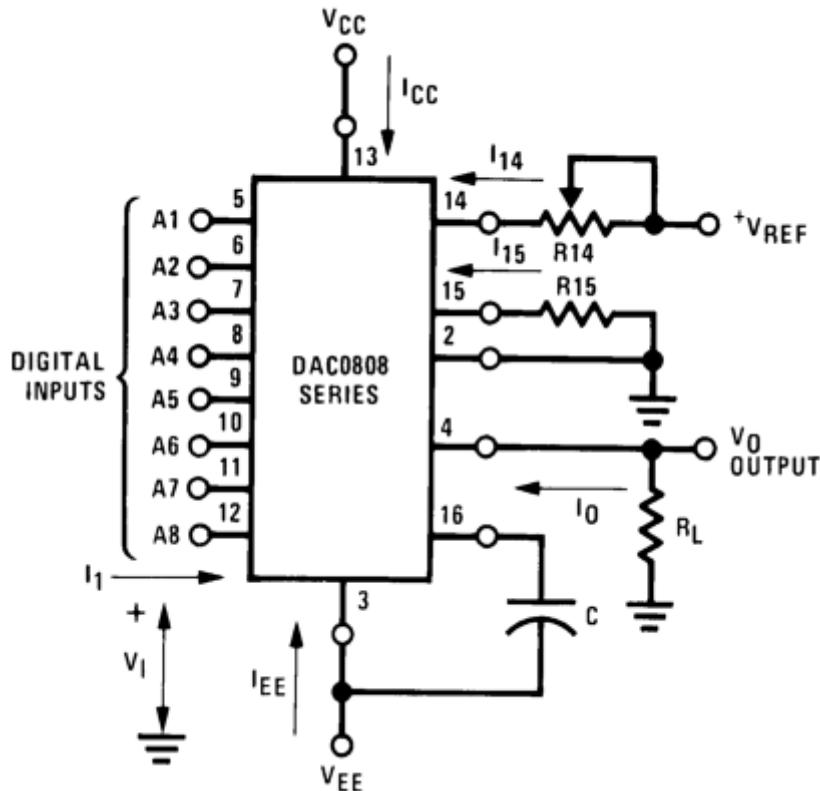
VARIANT 4:

- generator 8-bitowego słowa cyfrowego: projekt 8-bitowego licznika dwójkowego,
- precyzyjny woltomierz: miernik uniwersalny Agilent 34401A,
- sterowanie: ręcznie lub automatycznie obsługiwana płytka montażowa z licznikiem binarnym.

Jako 8-bitowy generator słowa cyfrowego wykorzystać należy odpowiednio połączone dwa 4-bitowe liczniki dwójkowe oparte na układzie TTL: 7493. Całość licznika zmontować na płycie montażowej. Generację zegara zapewnić wolnozmiennym generatorem przebiegu prostokątnego w standardzie TTL

lub synchronizacją ręczną. Obszerna informacja licznika dwójkowego zawarta jest w ćwiczeniu: *C-3. Liczniki asynchroniczne w technologii TTL, dwójkowe i dziesiętne.*

Jako alternatywę lub dodatkowy pomiar do ćwiczenia można wykorzystać komercyjny układ scalony 8-bitowego przetwornika cyfrowo-analogowego model **DAC0808** o wewnętrznej architekturze opartej na drabinie R-2R. Schemat połączeń przedstawia rysunek poniżej.



Rys. 7. Schemat przetwornika cyfrowo-analogowego DAC0808 do pomiarów podstawowych parametrów układu. Dane: $R_{14}=R_{15}=R_L=5\text{k}\Omega$, $C=100\text{nF}$, $+V_{ref}=10\text{V}$, $V_{CC}=+5\text{V}$, $V_{EE}=-15\text{V}$

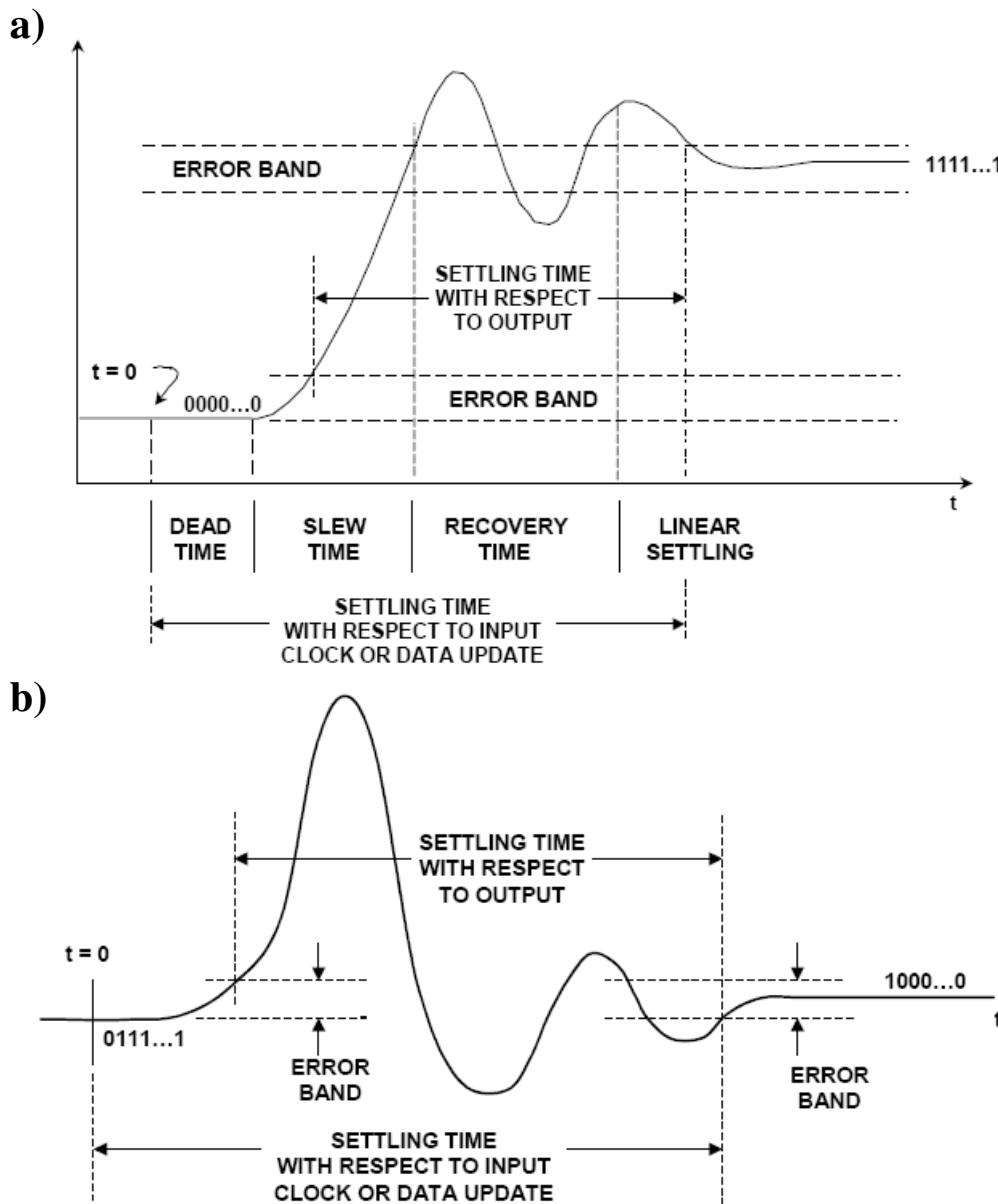
Opracowanie wyników:

Na podstawie pomiarów wyznaczyć:

- współczynnik skalowania V_{out} od słowa bitowego czyli wzmacnienie,
- wartość najmniej znaczącego bitu – LSB,
- pełny zakres napięcia wyjściowego,
- błąd wzmacnienia,
- przesunięcie zera (offset),
- błąd nieliniowości całkowej (wartość maksymalną oraz rozkład INL w funkcji słowa bitowego),
- błąd nieliniowości różniczkowej (wartość maksymalną oraz rozkład DNL w funkcji słowa bitowego),

2. Pomiar szybkości odpowiedzi przetwornika R-2R

Parametry szybkościowe (dynamiczne) graficznie przedstawione zostały na rys. 8.



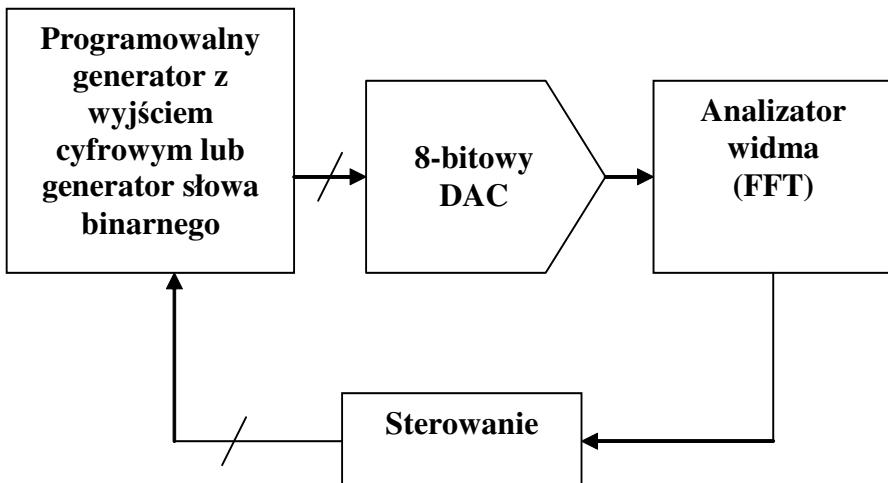
Rys. 8. Definicja parametru szybkości podpowiedzi przetwornika DAC. Dla zmiany o pełny zakres (a) oraz dla zmiany o LSB (b).

Pomiarów wykonać przy wykorzystaniu poprzedniego schematu testowego zamieniając precyzyjny voltmierz na oscyloskop.

W ćwiczeniu wykonać następujące punkty:

- zmieniając wartość słowa bitowego od 0 do wartości maksymalnej (255) zaobserwować szybkość zmian napięcia wyjściowego. Odczytać czas ustabilizowania się napięcia (*settling time with respect to input*),
- zmieniając wartość słowa bitowego o 1LSB zaobserwować szybkość zmian napięcia wyjściowego. Odczytać czas ustabilizowania się napięcia wyjściowego.

3. Pomiar zniekształceń i szumów



Rys. 9. Uproszczony schemat pomiaru zniekształceń i szumów przetwornika DAC.

Zaprogramować generator na wytwarzanie sygnału sinusoidalnego o częstotliwości f_0 . Słowo binarne podawane do wejścia DAC powinno zmieniać się od 0 do 255, proporcjonalnie do wartości chwilowej napięcia. Z pomiaru widma częstotliwościowego (prawidłowo dobrą spektrum FFT) wyznaczyć SINAD (signal-to-noise-and-distortion ratio) a następnie wyliczyć ENOB (effective number of bits) [6]:

$$SINAD = 20 \log_{10} \sqrt{(10^{-SNR/20})^2 + (10^{-THD/20})^2} \quad (1)$$

gdzie:

$$SNR[dB] = rms\ sygnału / rms\ szumów - 10 \log_{10} \left(\frac{M}{2} \right) \quad (1a)$$

gdzie: M – liczba binów procedury FFT

$$THD[dB] = 20 \log_{10} \sqrt{(10^{-V2/20})^2 + (10^{-V3/20})^2 + \dots + (10^{-V6/20})^2} \quad (1b)$$

$$ENOB = \frac{SINAD - 1.76dB}{6.02} \quad (2)$$

Literatura

1. K. Wawryń, R. Suszyński: Współczesne przetworniki a/c wykonywane w technologii CMOS. (Elektronika 2002)
2. Z. Kulka, M. Nadachowski, A. Libura: Przetworniki analogowo–cyfrowe i cyfrowo–analogowe
3. J. Zabrodzki, M. Łakomy Scalone przetworniki analogowo–cyfrowe i cyfrowo–analogowe. (Warszawa PWN 1992)
4. Kulka Z., Nadachowski M.: Liniowe układy scalone i ich zastosowanie.
5. Nota katalogowa układu DAC0808:
<http://www.ti.com/lit/ds/symlink/dac0808.pdf> zgodnie ze stanem na dzień 04.03.2013r.
6. *The Data Conversion Handbook*, Elsevier/Newnes, 2005, ISBN 0-7506-7841-0
7. ...

DAC0808

DAC0808 8-Bit D/A Converter



Literature Number: SNAS539A

DAC0808

8-Bit D/A Converter

General Description

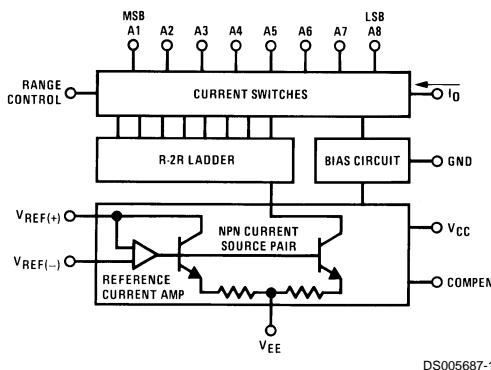
The DAC0808 is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with $\pm 5V$ supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ± 1 LSB of $255 I_{REF}/256$. Relative accuracies of better than $\pm 0.19\%$ assure 8-bit monotonicity and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC0808 is independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The DAC0808 will interface directly with popular TTL, DTL or CMOS logic levels, and is a direct replacement for the MC1508/MC1408. For higher speed applications, see DAC0800 data sheet.

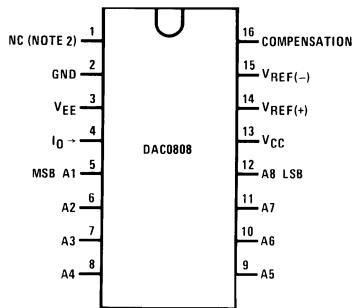
Features

- Relative accuracy: $\pm 0.19\%$ error maximum
- Full scale current match: ± 1 LSB typ
- Fast settling time: 150 ns typ
- Noninverting digital inputs are TTL and CMOS compatible
- High speed multiplying input slew rate: 8 mA/ μs
- Power supply voltage range: $\pm 4.5V$ to $\pm 18V$
- Low power consumption: 33 mW @ $\pm 5V$

Block and Connection Diagrams



DS005687-1

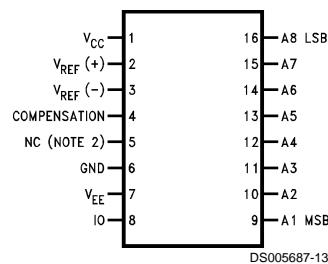
Dual-In-Line Package


DS005687-2

Top View
Order Number DAC0808
See NS Package M16A or N16A

Block and Connection Diagrams (Continued)

Small-Outline Package



Ordering Information

ACCURACY	OPERATING TEMPERATURE RANGE		
		N PACKAGE (N16A) (Note 1)	SO PACKAGE (M16A)
8-bit	0°C ≤ T _A ≤ +75°C	DAC0808LCN	MC1408P8
			DAC0808LCM

Note 1: Devices may be ordered by using either order number.

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage

V_{CC}	+18 V _{DC}
V_{EE}	-18 V _{DC}

Digital Input Voltage, V₅–V₁₂

-10 V_{DC} to +18 V_{DC}

Applied Output Voltage, V_O

-11 V_{DC} to +18 V_{DC}

Reference Current, I_{I_4}

5 mA

Reference Amplifier Inputs, V₁₄, V₁₅

V_{CC}, V_{EE}

Power Dissipation (Note 4)

1000 mW

ESD Susceptibility (Note 5)

TBD

Storage Temperature Range

-65°C to +150°C

Lead Temp. (Soldering, 10 seconds)

260°C

Dual-In-Line Package (Plastic)

300°C

Surface Mount Package

Vapor Phase (60 seconds) 215°C

Infrared (15 seconds) 220°C

Operating Ratings

Temperature Range

$T_{MIN} \leq T_A \leq T_{MAX}$

DAC0808

0 ≤ $T_A \leq +75^\circ\text{C}$

Electrical Characteristics

($V_{CC} = 5\text{V}$, $V_{EE} = -15\text{V}_{DC}$, $V_{REF}/R14 = 2\text{mA}$, and all digital inputs at high logic level unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
E_r	Relative Accuracy (Error Relative to Full Scale I_O) DAC0808LC (LM1408-8) Settling Time to Within ½ LSB (Includes t_{PLH})	(Figure 4) $T_A=25^\circ\text{C}$ (Note 7), (Figure 5)			±0.19	%
t_{PLH}, t_{PHL}	Propagation Delay Time	$T_A = 25^\circ\text{C}$, (Figure 5)		30	100	ns
TCI_O	Output Full Scale Current Drift			±20		ppm/°C
MSB	Digital Input Logic Levels High Level, Logic "1" Low Level, Logic "0"	(Figure 3)	2			
V_{IH}					0.8	V _{DC}
V_{IL}						V _{DC}
MSB	Digital Input Current High Level Low Level	(Figure 3) $V_{IH} = 5\text{V}$ $V_{IL} = 0.8\text{V}$		0 -0.003	0.040 -0.8	mA mA
I_{15}	Reference Input Bias Current	(Figure 3)		-1	-3	μA
	Output Current Range	(Figure 3) $V_{EE} = -5\text{V}$ $V_{EE} = -15\text{V}$, $T_A = 25^\circ\text{C}$	0 0	2.0 2.0	2.1 4.2	mA mA
I_O	Output Current	$V_{REF} = 2.000\text{V}$, $R14 = 1000\Omega$, (Figure 3)	1.9	1.99	2.1	mA
	Output Current, All Bits Low	(Figure 3)		0	4	μA
	Output Voltage Compliance (Note 3) $V_{EE} = -5\text{V}$, $I_{REF} = 1\text{mA}$ V_{EE} Below -10V	$E_r \leq 0.19\%$, $T_A = 25^\circ\text{C}$			-0.55, +0.4 -5.0, +0.4	V _{DC} V _{DC}
SRI _{REF}	Reference Current Slew Rate	(Figure 6)	4	8		mA/μs
	Output Current Power Supply Sensitivity	$-5\text{V} \leq V_{EE} \leq -16.5\text{V}$		0.05	2.7	μA/V
I_{CC} I_{EE}	Power Supply Current (All Bits Low)	(Figure 3)				
				2.3 -4.3	22 -13	mA mA
V_{CC} V_{EE}	Power Supply Voltage Range	$T_A = 25^\circ\text{C}$, (Figure 3)	4.5 -4.5	5.0 -15	5.5 -16.5	V _{DC} V _{DC}
	Power Dissipation					

Electrical Characteristics (Continued)

($V_{CC} = 5V$, $V_{EE} = -15V_{DC}$, $V_{REF}/R14 = 2\text{ mA}$, and all digital inputs at high logic level unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	All Bits Low	$V_{CC} = 5V$, $V_{EE} = -5V$		33	170	mW
	All Bits High	$V_{CC} = 5V$, $V_{EE} = -15V$ $V_{CC} = 15V$, $V_{EE} = -5V$ $V_{CC} = 15V$, $V_{EE} = -15V$		106 90 160	305	mW

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 3: Range control is not required.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} , θ_{JA} , and the ambient temperature, T_A . The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX} = 125^\circ C$, and the typical junction-to-ambient thermal resistance of the dual-in-line J package when the board mounted is $100^\circ C/W$. For the dual-in-line N package, this number increases to $175^\circ C/W$ and for the small outline M package this number is $100^\circ C/W$.

Note 5: Human body model, 100 pF discharged through a $1.5\text{ k}\Omega$ resistor.

Note 6: All current switches are tested to guarantee at least 50% of rated current.

Note 7: All bits switched.

Note 8: Pin-out numbers for the DAL080X represent the dual-in-line package. The small outline package pinout differs from the dual-in-line package.

Typical Application

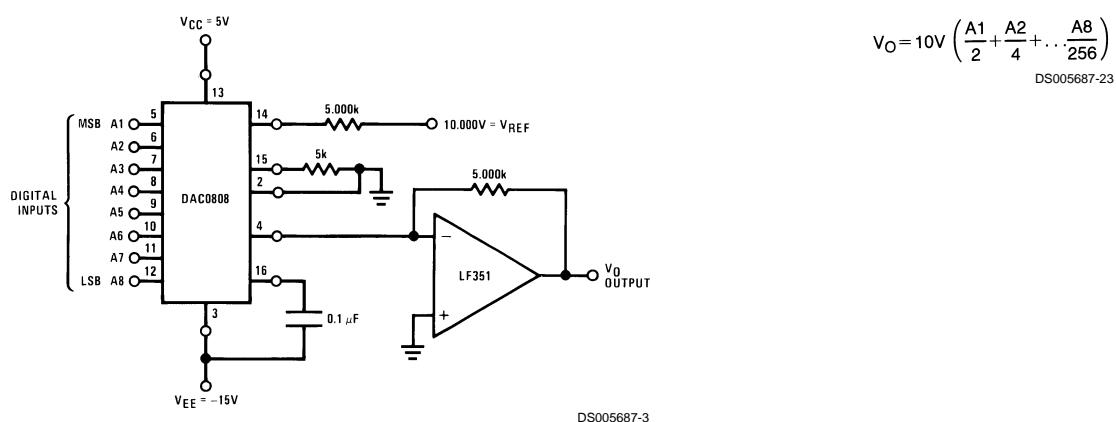
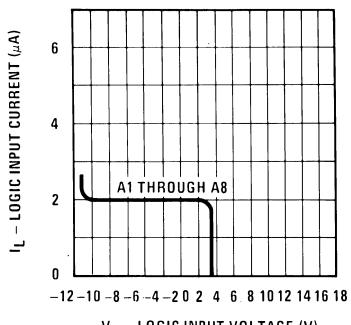


FIGURE 1. +10V Output Digital to Analog Converter (Note 8)

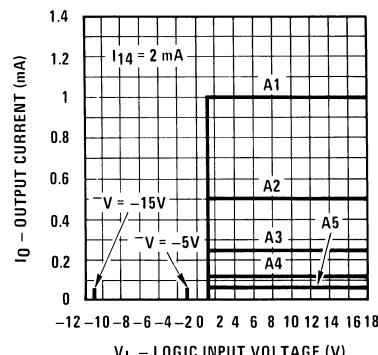
Typical Performance Characteristics

$V_{CC} = 5V$, $V_{EE} = -15V$, $T_A = 25^\circ C$, unless otherwise noted

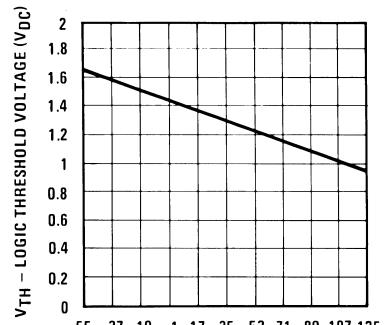
Logic Input Current vs Input Voltage



Bit Transfer Characteristics



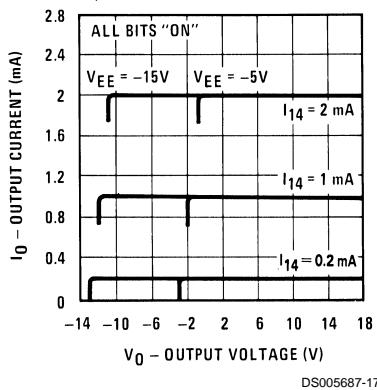
Logic Threshold Voltage vs Temperature



Typical Performance Characteristics

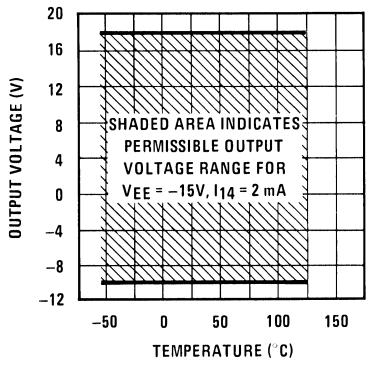
$V_{CC} = 5V$, $V_{EE} = -15V$, $T_A = 25^\circ C$, unless otherwise noted (Continued)

Output Current vs Output Voltage (Output Voltage Compliance)



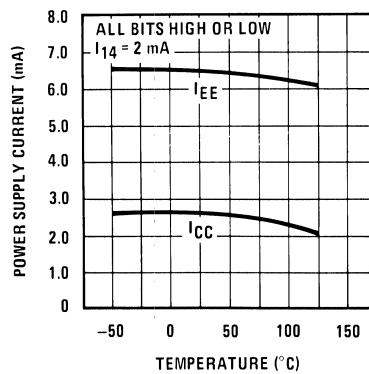
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Output Voltage Compliance vs Temperature



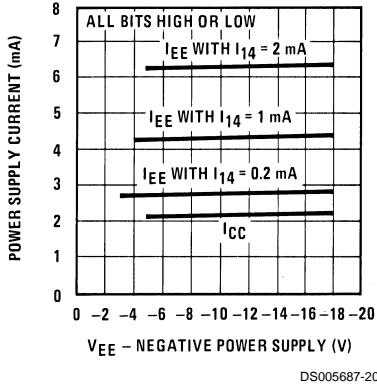
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Typical Power Supply Current vs Temperature



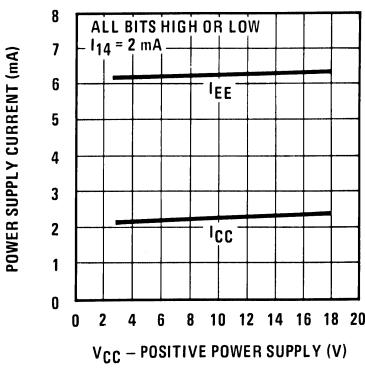
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Typical Power Supply Current vs V_{EE}



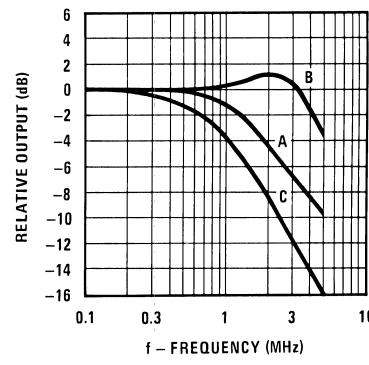
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Typical Power Supply Current vs V_{CC}



DS005687-21

Reference Input Frequency Response



DS005687-22

Unless otherwise specified: $R_{14} = R_{15} = 1\text{ k}\Omega$, $C = 15\text{ pF}$, pin 16 to V_{EE} ; $R_L = 50\Omega$, pin 4 to ground.

Curve A: Large Signal Bandwidth Method of Figure 7, $V_{REF} = 2\text{ Vp-p}$ offset 1V above ground.

Curve B: Small Signal Bandwidth Method of Figure 7, $R_L = 250\Omega$, $V_{REF} = 50\text{ mVp-p}$ offset 200 mV above ground.

Curve C: Large and Small Signal Bandwidth Method of Figure 9 (no op amp, $R_L = 50\Omega$), $R_S = 50\Omega$, $V_{REF} = 2V$, $V_S = 100\text{ mVp-p}$ centered at 0V.

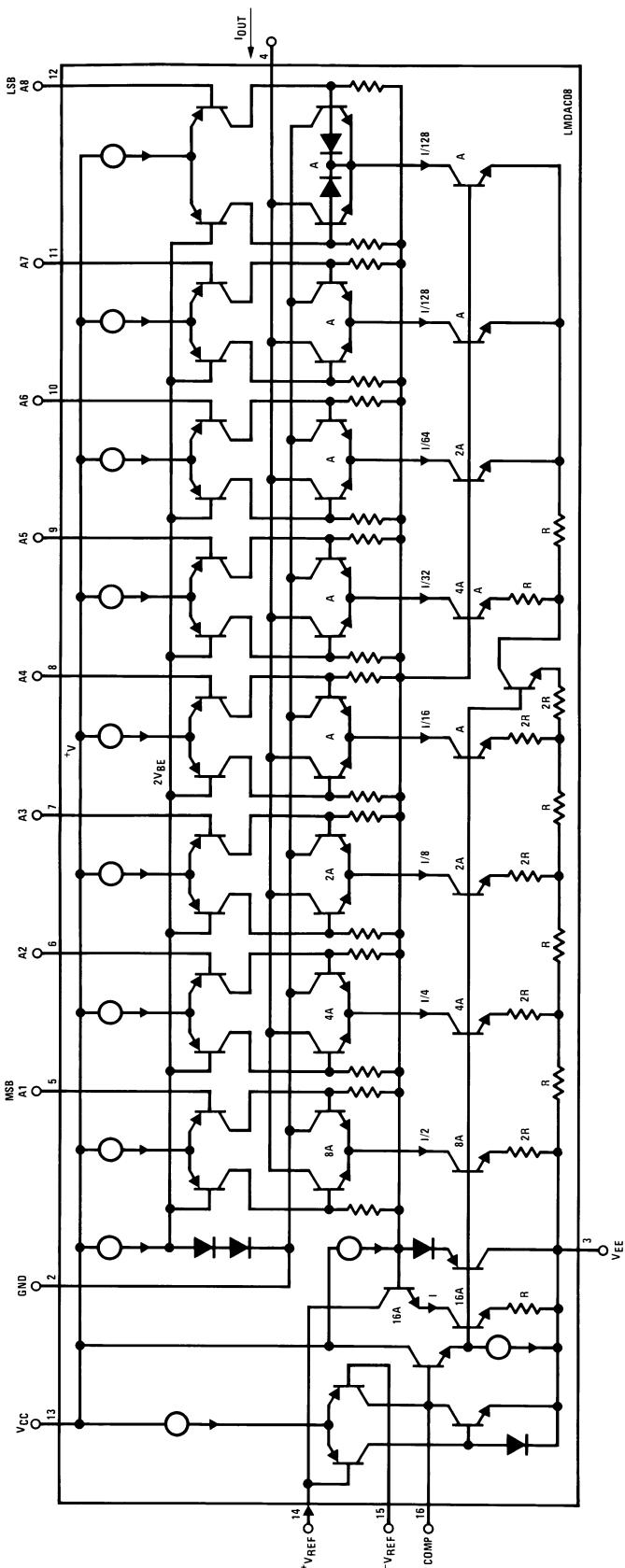
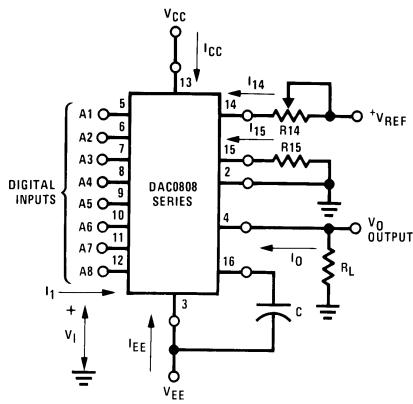


FIGURE 2. Equivalent Circuit of the DAC0808 Series (Note 8)

DS005687-4

Test Circuits



DS005687-6

V_1 and I_1 apply to inputs A1–A8.

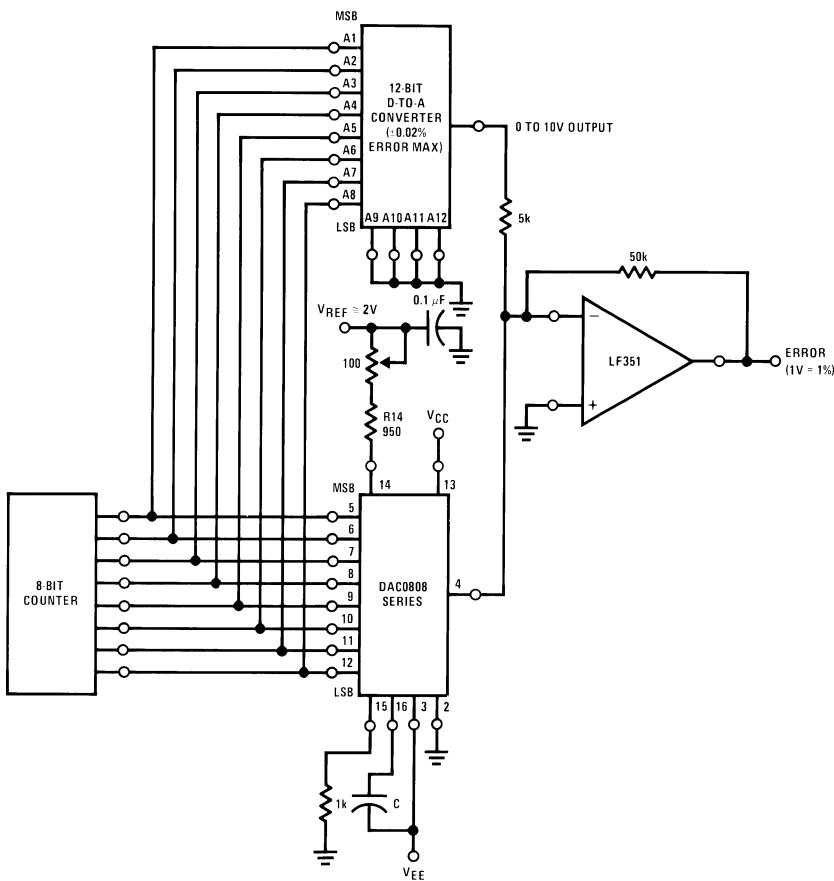
The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_0 = K \left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256} \right)$$

where $K \cong \frac{V_{REF}}{R14}$

and $A_N = "1"$ if A_N is at high level
 $A_N = "0"$ if A_N is at low level

FIGURE 3. Notation Definitions Test Circuit (Note 8)



DS005687-7

FIGURE 4. Relative Accuracy Test Circuit (Note 8)

Test Circuits (Continued)

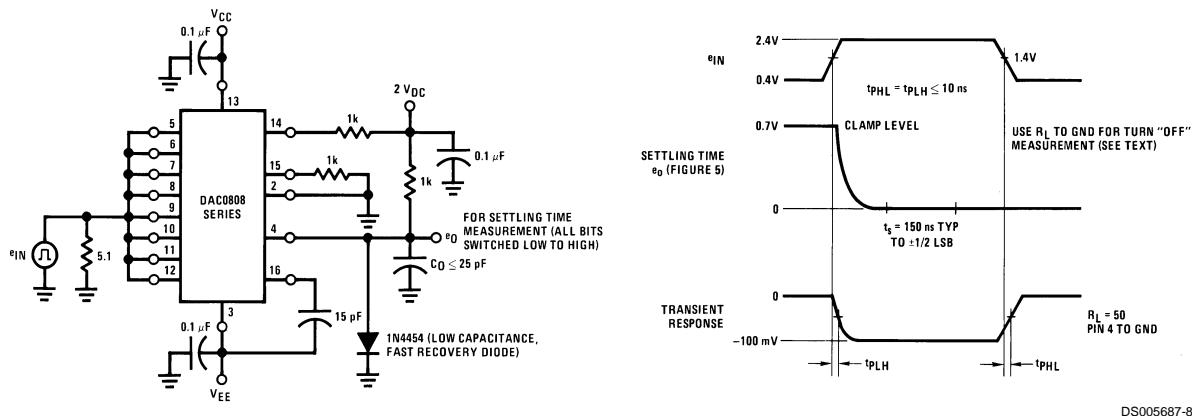


FIGURE 5. Transient Response and Settling Time (Note 8)

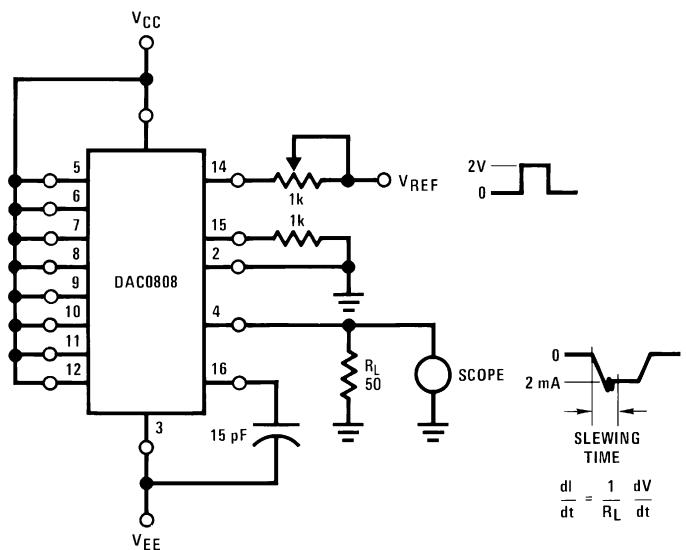


FIGURE 6. Reference Current Slew Rate Measurement (Note 8)

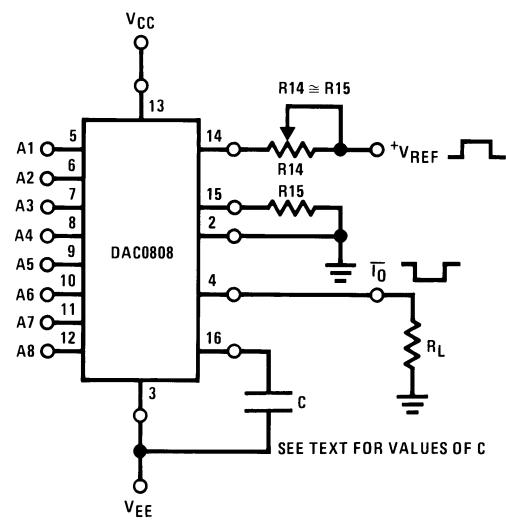


FIGURE 7. Positive \$V_{REF}\$ (Note 8)

Test Circuits (Continued)

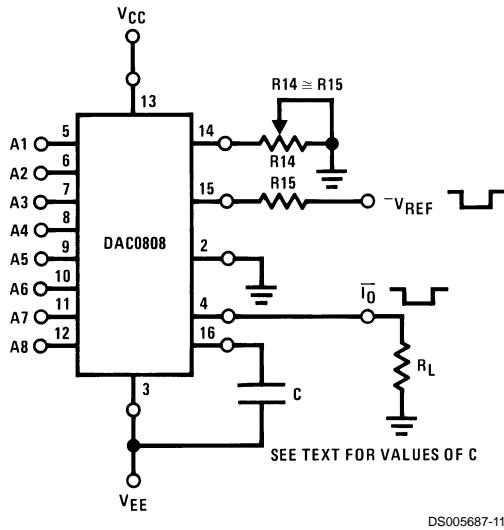


FIGURE 8. Negative V_{REF} (Note 8)

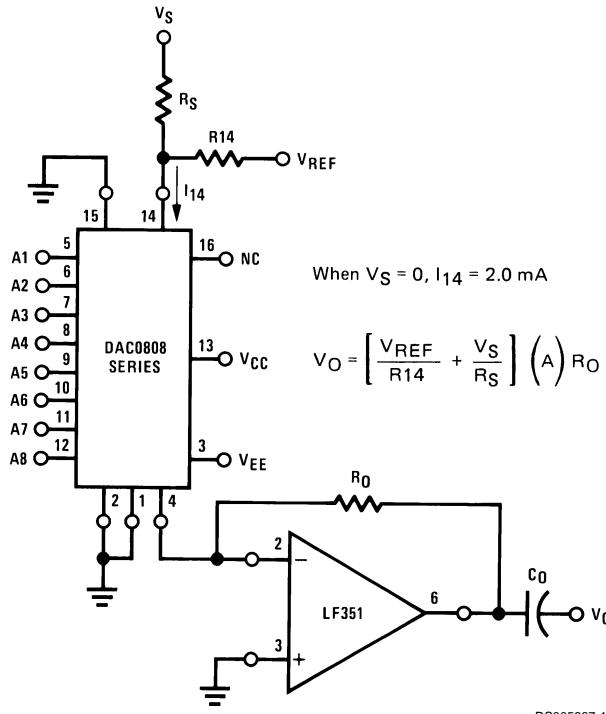


FIGURE 9. Programmable Gain Amplifier or Digital Attenuator Circuit (Note 8)

Application Hints

REFERENCE AMPLIFIER DRIVE AND COMPENSATION

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I_{14} , must always flow into pin 14, regardless of the set-up method or reference voltage polarity.

Connections for a positive voltage are shown in *Figure 7*. The reference voltage source supplies the full current I_{14} .

For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1, 2.5 and 5 k Ω , minimum capacitor values are 15, 37 and 75 pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in *Figure 8*. A high input impedance is the main

Application Hints (Continued)

advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 4V above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to 5V through another resistor and bypassing the junction of the 2 resistors with 0.1 μ F to ground. For reference voltages greater than 5V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

OUTPUT VOLTAGE RANGE

The voltage on pin 4 is restricted to a range of -0.55 to 0.4V when $V_{EE} = -5V$ due to the current switching methods employed in the DAC0808.

The negative output voltage compliance of the DAC0808 is extended to -5V where the negative supply voltage is more negative than -10V. Using a full-scale current of 1.992 mA and load resistor of 2.5 k Ω between pin 4 and ground will yield a voltage output of 256 levels between 0 and -4.980V. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500 Ω do not significantly affect performance, but a 2.5 k Ω load increases worst-case settling time to 1.2 μ s (when all bits are switched ON). Refer to the subsequent text section on Settling Time for more details on output loading.

OUTPUT CURRENT RANGE

The output current maximum rating of 4.2 mA may be used only for negative supply voltages more negative than -8V, due to the increased voltage drop across the resistors in the reference current amplifier.

ACCURACY

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current. The relative accuracy of the DAC0808 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder.

The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC0808 has a very low full-scale current drift with temperature.

The DAC0808 series is guaranteed accurate to within $\pm 1/2$ LSB at a full-scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2 mA, with the loss of 1 LSB (8 μ A) which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in *Figure 4*. The 12-bit converter is calibrated for a full-scale output current of 1.992 mA. This is an optional step since the DAC0808 accuracy is essentially the same between 1.5 and 2.5 mA. Then the DAC0808 circuits' full-scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accuracy D-to-A converter. 16-bit accuracy implies a total error of $\pm 1/2$ of one part in 65,536 or $\pm 0.00076\%$, which is much more accurate than the $\pm 0.019\%$ specification provided by the DAC0808.

MULTIPLYING ACCURACY

The DAC0808 may be used in the multiplying mode with 8-bit accuracy when the reference current is varied over a range of 256:1. If the reference current in the multiplying mode ranges from 16 μ A to 4 mA, the additional error contributions are less than 1.6 μ A. This is well within 8-bit accuracy when referred to full-scale.

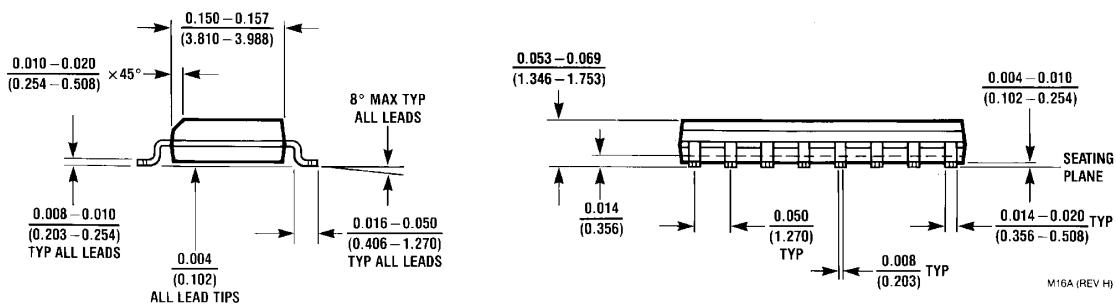
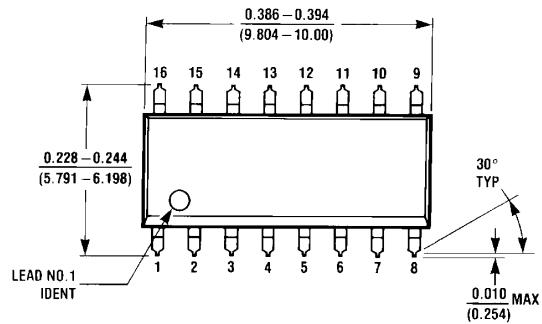
A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the DAC0808 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a DC reference current is 0.5 to 4 mA.

SETTLING TIME

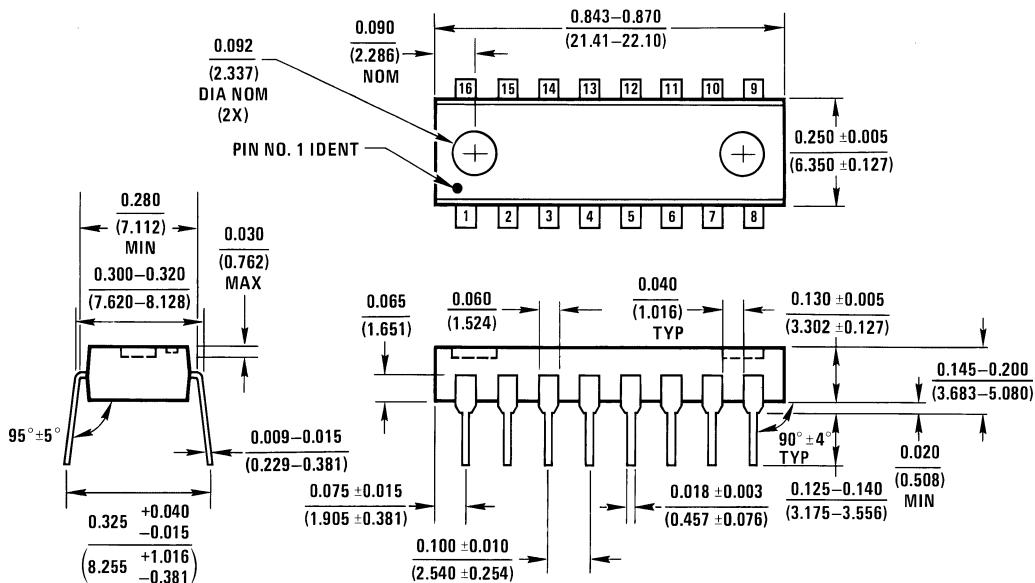
The worst-case switching condition occurs when all bits are switched ON, which corresponds to a low-to-high transition for all bits. This time is typically 150 ns for settling to within $\pm 1/2$ LSB, for 8-bit accuracy, and 100 ns to $1/2$ LSB for 7 and 6-bit accuracy. The turn OFF is typically under 100 ns. These times apply when $R_L \leq 500\Omega$ and $C_O \leq 25 \text{ pF}$.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100 μ F supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

Physical Dimensions inches (millimeters) unless otherwise noted



Small Outline Package
Order Number DAC0808LCM
NS Package Number M16A



Dual-In-Line Package
Order Number DAC0808
NS Package Number N16A

Notes

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